LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A P-channel MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having substantially flat, parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;

at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;

a gate electrode comprised of polysilicon implanted with p-type ~~polysilicon~~ dopants disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode said gate being insulated from said channel region by a gate oxide layer comprising silicon dioxide, said gate oxide layer being comprised of radiation hardened silicon dioxide and less than 1000Å thick;

an interlayer oxide disposed over each gate electrode and having tapered profile portions each aligned with a respective P-type source region; and

a source electrode disposed atop said upper surface and connected to said at least one P-type source region;

wherein said gate oxide is capable of resisting threshold voltage shift due to total radiation dose and capable of resisting single event gate rupture due to a single event effect.

2. (canceled).

3. (original) The MOS gated device of claim 2 wherein said gate dielectric has a thickness of between 500 to 1000Å.

4. (previously presented) The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about $5.5x10^{13}$ atoms/cm^2.

5. (previously presented) The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about $8.0x10^{13}$ atoms/cm^2.

6. (original) The MOS gated device of claim 1 wherein said substrate includes a chip of monocrystalline silicon at said lower surface of said substrate and an epitaxial layer formed atop said chip and that is less heavily doped than said chip.

7. (previously presented) The MOS gated device of claim 1 wherein at least one of said N-type body regions includes a portion adjacent to said upper surface that is more heavily doped than another portion of said N-type body regions that is adjacent to a lower boundary between said N-type body region and said substrate.

8. (canceled).

9. (currently amended) The MOS gated device of claim 1 wherein said interlayer oxide ~~dielectric~~ is low temperature oxide.

10. (canceled).

11. (original) The MOS gated device of claim 1 further comprising a passivation layer formed atop said source electrode.

12. (original) The MOS gated device of claim 11 wherein said passivation layer is comprised of low temperature oxide.

13. (previously presented) The MOS gated device of claim 1 wherein said gate electrode has a doping concentration corresponding to that of an approximately 50 KeV boron implant of about $5x10^{15}$ atoms/cm^2.

Claims 14-31 (canceled).